CD4511B Types

CMOS BCD-to-7-Segment Latch Decoder Drivers

High-Voltage Types (20-Volt Rating)
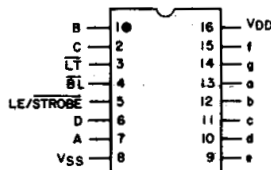
DISPLAY

92CS-25087

FUNCTIONAL DIAGRAM

■ CD4511B types are BCD-to-7-segment latch decoder drivers constructed with CMOS logic and n-p-n bipolar transistor output devices on a single monolithic structure. These devices combine the low quiescent power dissipation and high noise immunity features of RCA CMOS with n-p-n bipolar output transistors capable of sourcing up to 25 mA. This capability allows the CD4511B types to drive LED's and other displays directly.
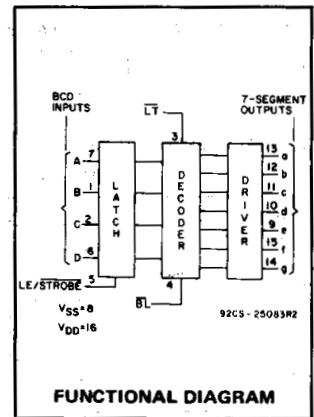
Lamp Test ($\overline{LT}$), Blanking ($\overline{BL}$), and Latch Enable or Strobe inputs are provided to test the display, shut off or intensity-modulate it, and store or strobe a BCD code, respectively. Several different signals may be multiplexed and displayed when external multiplexing circuitry is used.

The CD4511B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

These devices are similar to the type MC14511.

Features:

■ High-output-sourcing capability . . . . up to 25 mA
■ Input latches for BCD Code storage
■ Lamp Test and Blanking capability
■ 7-segment outputs blanked for BCD input codes > 1001
■ 100% tested for quiescent current at 20 V
■ Max. input current of 1 μA at 18 V, over full package-temperature range, 100 nA at 18 V and 25°C
■ 5-V, 10-V, and 15-V parametric ratings

Applications:

■ Driving common-cathode LED displays
■ Multiplexing with common-cathode LED displays
■ Driving incandescent displays
■ Driving low-voltage fluorescent displays

TERMINAL ASSIGNMENT (CD4511B, TOP VIEW)

Pin		Pin
B — 1		16 — VDD
C — 2		15 — f
$\overline{LT}$ — 3		14 — g
$\overline{BL}$ — 4		13 — a
LE/STROBE — 5		12 — b
D — 6		11 — c
A — 7		10 — d
VSS — 8		9 — e

TOP VIEW

92CS-25084RI

CD4511B TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) . . . . -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT . . . . ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C . . . . Derate Linearily at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) . . . . -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

Characteristic	V_{DD}	Min.	Max.	Units
Supply-Voltage Range (T_A): (Full Package-Temperature Range)	–	3	18	V
Set-Up Time (t_S)	5	150	–	ns
	10	70	–	ns
	15	40	–	ns
Hold Time (t_H)	5	0	–	ns
	10	0	–	ns
	15	0	–	ns
Strobe Pulse Width (t_W)	5	400	–	ns
	10	160	–	ns
	15	100	–	ns

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS				LIMITS AT INDICATED TEMPERATURES (°C)							Units
	I_{OH} (mA)	V_o (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current: I_{DD} Max.	−	−	−	5	5	5	150	150	−	0.04	5	μA
	−	−	−	10	10	10	300	300	−	0.04	10	
	−	−	−	15	20	20	600	600	−	0.04	20	
	−	−	−	20	100	100	3000	3000	−	0.08	100	
Output Voltage: Low-Level V_{OL} Max.	−	−	0.5	5	0.05				−	0	0.05	V
	−	−	0.10	10	0.05				−	0	0.05	
	−	−	0.15	15	0.05				−	0	0.05	
High-Level V_{OH} Min.	−	−	0.5	5	4	4	4.2	4.2	4.1	4.55	−	V
	−	−	0.10	10	9	9	9.2	9.2	9.1	9.55	−	
	−	−	0.15	15	14	14	14.2	14.2	14.1	14.55	−	
Input Low Voltage, V_{IL} Max.	−	0.5,3.8		5	1.5				−	−	1.5	V
	−	1,8.8	−	10	3				−	−	3	
		1.5,13.8		15	4				−	−	4	
Input High Voltage, V_{IH} Min.	−	0.5,3.8		5	3.5				3.5	−	−	V
	−	1,8.8		10	7				7	−	−	
		1.5,13.8		15	11				11	−	−	
Output Drive Voltage: High Level V_{OH} Min.	0			5	4.0	4.0	4.20	4.20	4.10	4.55	−	V
	5	−					−	−	−	4.25	−	
	10				3.80	3.80	3.90	3.90	3.90	4.10	−	
	15						3.50	3.50	−	3.95	−	
	20				3.55	3.55	3.30	−	3.40	3.75	−	
	25				3.40	3.40	−	−	3.10	3.55	−	
	0		−	10	9.0	9.0	9.20	9.20	9.10	9.55	−	V
	5				−	−	−	−	−	9.25	−	
	10	−	−		8.85	8.85	9.00	9.00	9.00	9.15	−	
	15	−	−		−	−	−	−	−	9.05	−	
	20	−	−		8.70	8.70	8.40	8.40	8.60	8.90	−	
	25	−	−		8.60	8.60	−	−	8.30	8.75	−	
	0	−	−	15	14.0	14.0	14.20	14.20	14.10	14.55	−	V
	5	−	−		−	−	−	−	−	14.30	−	
	10	−	−		13.90	13.90	14.0	14.0	14.0	14.20	−	
	15	−	−		−	−	−	−	−	14.10	−	
	20	−	−		13.75	13.75	13.50	13.50	13.70	13.95	−	
	25	−	−		13.65	13.65	−	−	13.50	13.80	−	
Output Low (Sink) Current, I_{OL} Min.	−	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	−	mA
	−	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	−	
	−	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	−	
Input Current, I_{IN} Max.	−	0,18	0,18	18	±0.1	±0.1	±1	±1	−	±10⁻⁵	±0.1	μA

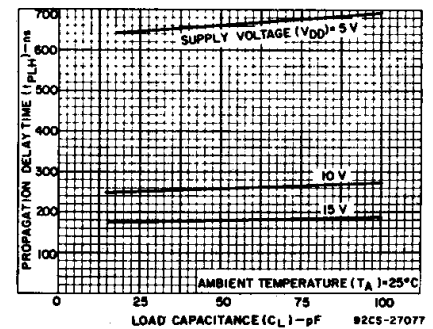Fig. 1 — Typical output low (sink) current characteristics.

Fig. 2 — Typical data-to-output, low-to-high-level propagation delay time as a function of load capacitance.

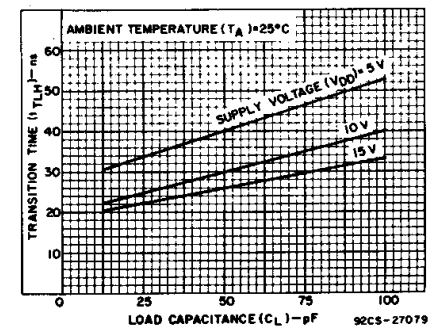Fig. 3 — Typical data-to-output, high-to-low-level propagation delay time as a function of load capacitance.

Fig. 4 — Typical low-to-high-level transition time as a function of load capacitance.

CD4511B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, Input t_r, t_f = 20 ns,
  C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	Test Conditions V_{DD} Volts	LIMITS All Packages Min.	Typ.	Max.	UNITS
Propagation Delay Time: (Data) High-to-Low Level, t_{PHL}	5	–	520	1040	
	10	–	210	420	ns
	15	–	150	300	
Low-to-High Level, t_{PLH}	5	–	660	1320	
	10	–	260	520	ns
	15	–	180	360	
Propagation Delay Time: (BL) High-to-Low Level, t_{PHL}	5	–	350	700	
	10	–	175	350	ns
	15	–	125	250	
Low-to-High Level, t_{PLH}	5	–	400	800	
	10	–	175	350	ns
	15	–	150	300	
Propagation Delay Time: (LT) High-to-Low Level, t_{PHL}	5	–	250	500	
	10	–	125	250	ns
	15	–	85	170	
Low-to-High Level, t_{PLH}	5	–	150	300	
	10	–	75	150	ns
	15	–	50	100	
Transition Time: Low-to-High Level, t_{TLH}	5	–	40	80	
	10	–	30	60	ns
	15	–	25	50	
High-to-Low Level, t_{THL}	5	–	125	310	
	10	–	75	185	ns
	15	–	65	160	
Minimum Set-Up Time, t_S	5	150	75	–	
	10	70	35	–	ns
	15	40	20	–	
Minimum Hold Time, t_H	5	0	–75	–	
	10	0	–35	–	ns
	15	0	–20	–	
Strobe Pulse Width, t_W	5	400	200	–	
	10	160	80	–	ns
	15	100	50	–	
Input Capacitance, C_{IN}		–	5	7.5	pF

Fig. 5 – Typical high-to-low transition time as a function of load capacitance.

Fig. 6 – Typical voltage drop (V_{DD} to output) vs. output source current as a function of supply.
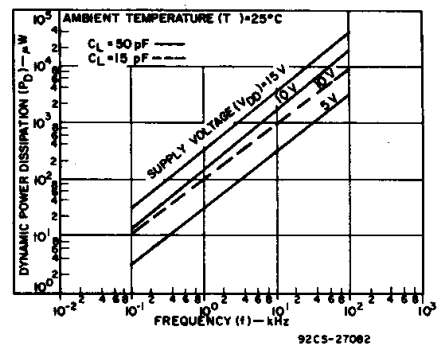
Fig. 7 – Typical dynamic power dissipation characteristics.

COMMERCIAL CMOS HIGH VOLTAGE ICs

3

Fig. 8 — Logic diagram.

TRUTH TABLE

LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X				*				*

X ≡ Don't Care   * Depends on BCD code previously applied when LE = 0

Note: Display is blank for all illegal input codes (BCD > 1001).

TEST CIRCUITS

Fig. 9 — Quiescent device current.
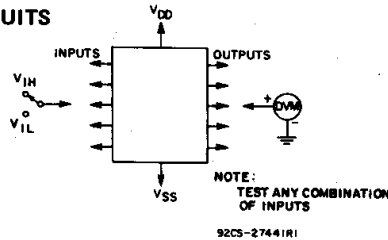
Fig. 10 — Input voltage.
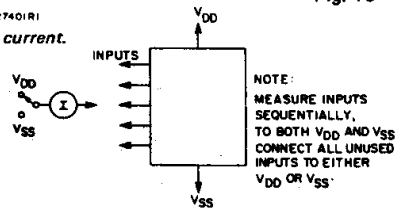
Fig. 11 — Input current.
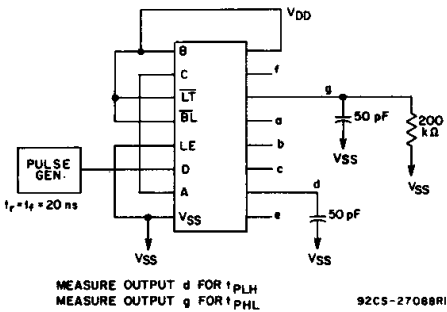
Fig. 12 — Data propagation delay.

MEASURE OUTPUT d FOR t_{PLH}
MEASURE OUTPUT g FOR t_{PHL}
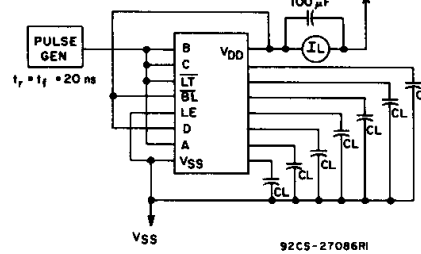
Fig. 13 — Dynamic power dissipation.
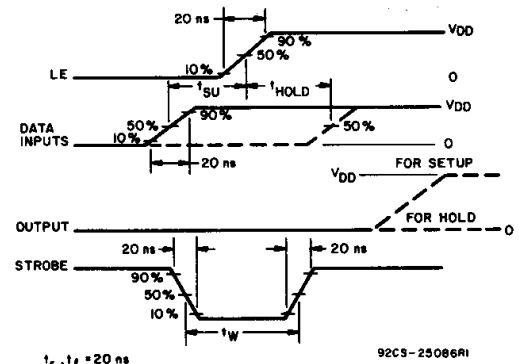
Fig. 14 — Dynamic waveforms.

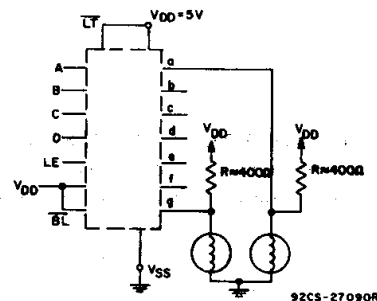## APPLICATIONS
Interfacing with Various Displays

92CS-27089RI

Duty Cycle = 100%

$I_{SEG} = I_{DIODE_{AVG.}} = 20$ mA at Luminous Intensity/Segment = 250 microcandles

$$R = \frac{V_{OH} - V_{DF}}{I_{SEG}}$$

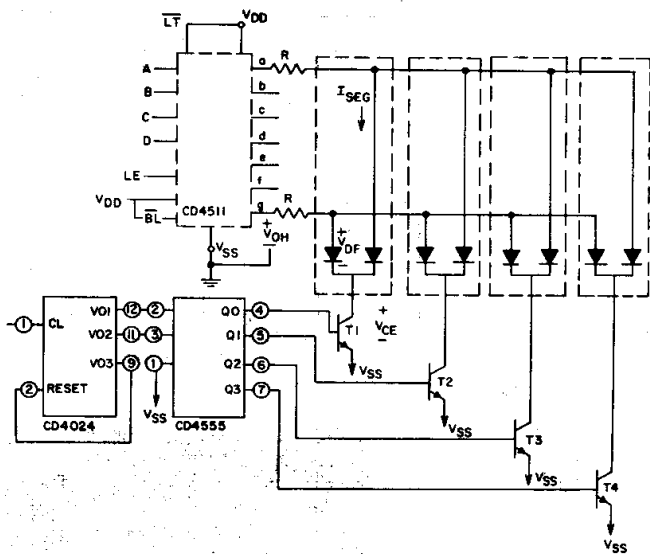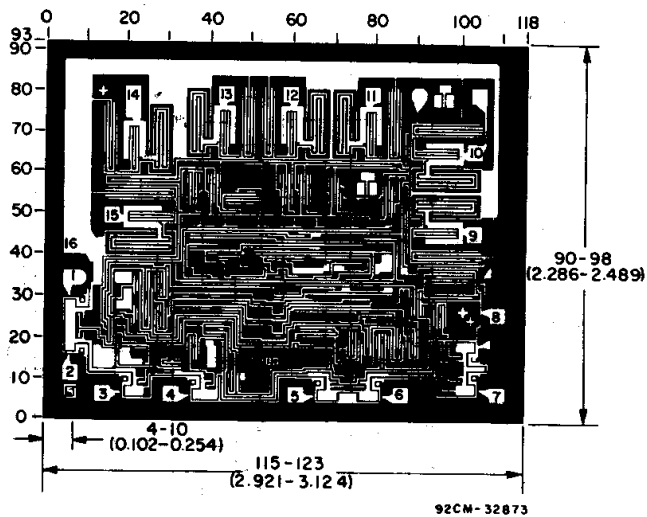Fig. 15 - Driving common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7740).

92CM-27087RI

Multiplexing Scheme Showing 2 of 7 Segments Connected

Transistors $T_1 - T_4$ (RCA-2N3053 or 2N2102) have I_C Max. rating $> 7 \times I_{SEG}$

Duty Cycle = 25%

$I_{SEG} = [I_{DIODE_{AVG}}] \times 4$

$$R = \frac{(V_{OH} - V_{DF} - V_{CE})}{I_{SEG}}$$

All unused inputs on CD4555
are connected to V_{DD} or V_{SS}.

Fig. 18 - Multiplexing with common-cathode 7-segment LED displays (example Hewlet-Packard 5082-7404 4 character display or 4 discrete Monosanto Man 3 displays).

92CS-2709IRI

A medium-brightness intensity display can be obtained with low-voltage fluorescent displays such as the Tung-Sol Digivac S/G** Series.

**Trademark Tung-Sol Division Wagner Electric Co.

Fig. 16 - Driving low-voltage fluorescent displays.

92CS-27090RI

2 of 7 Segments Shown Connected

Resistors R from V_{DD} to each 7-segment driver output are chosen to keep all Numitron segments slightly on and warm.

Fig. 17 - Driving incandescent displays (RCA Numitron DR2000 series displays).

92CM-32873

Dimensions and pad layout for CD4511B chip.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
CD4511BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4511BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4511BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4511BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type
CD4511BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4511BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4511BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4511BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4511BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4511BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

1   7

0.065 (1,65)
0.045 (1,14)

C

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°–15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

N (R−PDIP−T**)   PLASTIC DUAL−IN−LINE PACKAGE
16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14)

0.045 (1,14)
0.030 (0,76)

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
         D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
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PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

16   9

△D 4,50
    4,30

6,60
6,20

0,15 NOM

Gage Plane

0,25

1   8

0°−8°

5,10
4,90

△C

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ | 0,10

4040064−4/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B. This drawing is subject to change without notice.
         △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
             not exceed 0,15 each side.
         △D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E. Falls within JEDEC MO−153

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

→| |← 14x0,65

5,60

Stencil Openings
(Note D)

→| |← 16x0,30

16x1,55

→| |← 14x0,65

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

←0,35→

1,60

←0,07→
All Around

Example
Solder Mask Opening
(See Note E)

4211284−3/E 07/12

NOTES: A. All linear dimensions are in millimeters.
          B. This drawing is subject to change without notice.
          C. Publication IPC−7351 is recommended for alternate designs.
          D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
              contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

IMPORTANT NOTICE

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