HT8955A
Voice Echo

Features

- Operating voltage: 5.0V
- Long delay time
  - 0.8 seconds (SEL=VSS, 256K DRAM)
  - 0.2 seconds (SEL=VDD/open, 64K DRAM)
- 25KHz sampling rate
- Continuous variable delay time
- A built-in pre-amplifier
- Low distortion
- High S/N ratio
- Wide frequency response
- PCM 10 bit A/D and D/A converters
- 24 pin DIP package

Applications

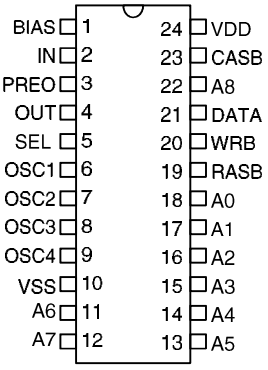
- Mixers
- Karaoke systems
- Echo generators
- Sound effect generators

General Description

The HT8955A is a CMOS LSI of a digital audio signal delay processor. It is designed for applications on audio systems including echo generators, Karaoke systems, sound effect generators, etc.

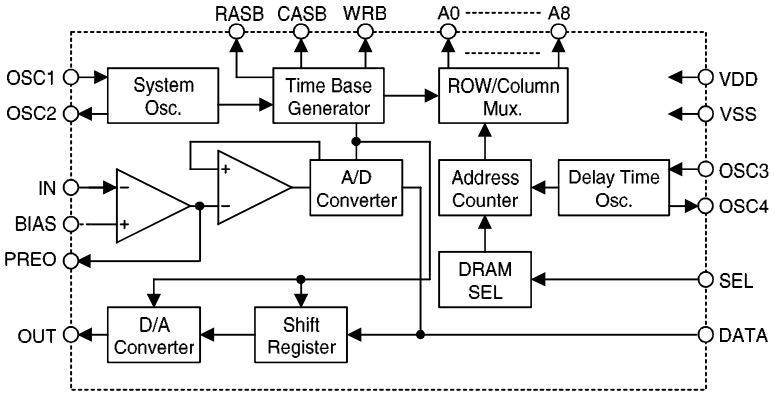
The LSI consists of a built-in pre-amplifier, on-chip oscillator, DRAM interface, 10 bit A/D and D/A converters as well as control logic. It provides continuously adjustable delay time up to 0.8/0.2 seconds at a sampling rate of 25KHz when combined with an external DRAM (41256/4164). The HT8955A is superior to an conventional BBD delay unit in its low distortion, high S/N ratio in addition to long delay time. Its sophisticated low pass filter will not end in normal applications due to a high sampling rate (25~50KHz). Given this, the HT8955A is excellent for applications on audio delay systems. It is offered in a 24 pin dual-in-line package.

Pin Assignment



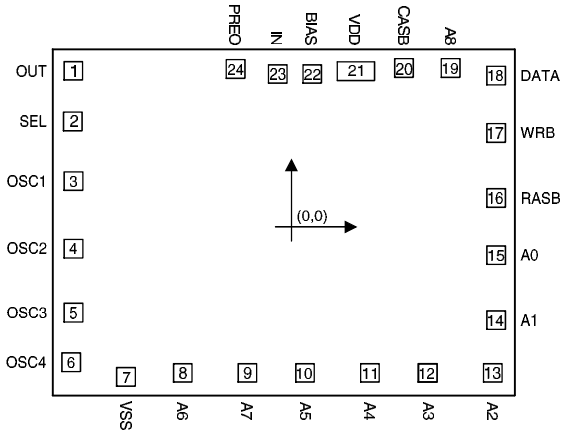
HT8955A
– 24 DIP

Block Diagram



Pad Coordinates

Unit: μm



Pad No.	X	Y	Pad No.	X	Y
1	–1138.00	796.50	14	1141.50	–547.00
2	–1141.00	523.50	15	1141.50	–197.50
3	–1136.50	201.50	16	1141.50	111.50
4	–1136.50	–163.00	17	1141.50	461.00
5	–1137.00	–507.00	18	1141.50	770.50
6	–1149.00	–774.00	19	896.00	811.00
7	–854.50	–853.50	20	645.00	810.50
8	–548.00	–831.50	21	435.00	794.00
9	–198.50	–831.50	21	335.00	794.00
10	111.50	–831.50	22	150.00	779.00
11	461.00	–831.50	23	–35.00	779.00
12	773.00	–831.50	25	–264.00	806.00
13	1122.50	–831.50			

Chip size: $2170 \times 2200\ (\mu m)^2$

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pin Description

Pin No.	Pin Name	I/O	Internal Connection	Description
1	BIAS	O	OP Non-inverting	Bias of an internal pre-amplifier It connects to a decoupling capacitor.
2	IN	I	OP Inverting	Audio signal input pin (inverting)
3	PREO	O	OP Output	Pre-amplifier output pin
4	OUT	O	—	Delayed audio signal output pin
5	SEL	I	Pull-High	DRAM type selection: VDD or Open: 64Kb VSS: 256Kb
6	OSC1	I	—	System oscillator input
7	OSC2	O	—	System oscillator output
8	OSC3	I	—	Delay time control oscillator input
9	OSC4	O	—	Delay time control oscillator output
10	VSS	I	—	Negative power supply (GND)
11	A6	O	CMOS Out	It connects to DRAM A6.
12	A7	O	CMOS Out	It connects to DRAM A7.

Pin No.	Pin Name	I/O	Internal Connection	Description
13	A5	O	CMOS Out	It connects to DRAM A5.
14	A4	O	CMOS Out	It connects to DRAM A4.
15	A3	O	CMOS Out	It connects to DRAM A3.
16	A2	O	CMOS Out	It connects to DRAM A2.
17	A1	O	CMOS Out	It connects to DRAM A1.
18	A0	O	CMOS Out	It connects to DRAM A0.
19	RASB	O	CMOS Out	It connects to DRAM RASB.
20	WRB	O	CMOS Out	It connects to DRAM WRB.
21	DATA	I/O	CMOS I/O	Data I/O pin
22	A8	O	CMOS I/O	It connects to DRAM A8.
23	CASB	O	CMOS I/O	It connects to DRAM CASB.
24	VDD	I	—	Positive power supply

Absolute Maximum Ratings

Supply Voltage ..... –0.3V to 6V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature..... –50°C to 125°C
Operating Temperature..... –20°C to 70°C

Electrical Characteristics

(Ta=25°C)

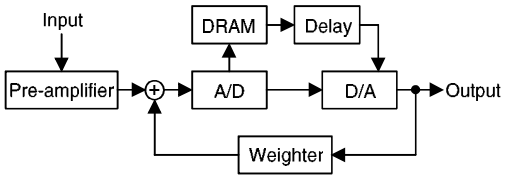
Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
V_{DD}	Operating Voltage	—	—	4.5	5.0	5.5	V
I_{OP}	Operating Current	5V	No load, F_{OSC}=640KHz	—	2.5	8	mA
A_V	Pre-amplifier Voltage Gain	5V	R_L>100KΩ Open loop	—	2000	—	V/V
A_V	Comparator Voltage Gain	5V	R_L>100KΩ Open loop	—	2000	—	V/V
V_{IL}	"L" Input Voltage	—	—	0	—	$0.3V_{DD}$	V
V_{IH}	"H" Input Voltage	—	—	$0.7V_{DD}$	—	V_{DD}	V
V_{OMAX}	Maximum Output Voltage	5V	R_L>470KΩ	1	1.5	—	V

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V_{DD}	Condition				
Td	Maximum Delay Time	5V	SEL=open, 25KHz sampling rate	0.15	0.2	—	s
Td		5V	SEL=VSS, 25KHz sampling rate	0.6	0.8	—	s
S/N	Signal to Noise Ratio	5V	V_O=1V, 400Hz BW=10KHz	—	55	—	dB
THD	Total Harmonic Distortion	5V	V_O=1V, 400Hz BW=7KHz	—	0.5	—	%

Functional Description

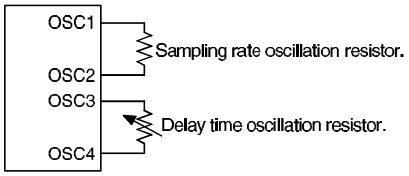
The HT8955A is a single chip LSI with an external DRAM. It is designed for processing audio signal delay. The LSI includes a built-in pre-amplifier, 10 bit A/D and D/A converters. The A/D and D/A converters ensure a low distortion as well as a high S/N ratio of the audio delay system. The LSI, in addition, provides 2 sets of oscillation circuit for system sampling rate and audio echo delay time.

Playing function block diagram



System oscillator

The HT8955A provides 2 oscillator for sampling rate and echo delay time individually. The oscillator of sampling rate requires an external resistor between the OSC1 and OSC2 pins. A higher sampling rate (25~50KHz) can thus be derived by adjusting the oscillation resistor without a sophisticated low pass filter. The oscillator of delay time, on the other hand, demands an external resistor between the OSC3 and OSC4 pins. By altering the oscillation resistor, its delay time can be continuously adjusted up to 0.8/0.2 seconds at a 25KHz sampling rate for DRAM of 256Kb/64Kb.



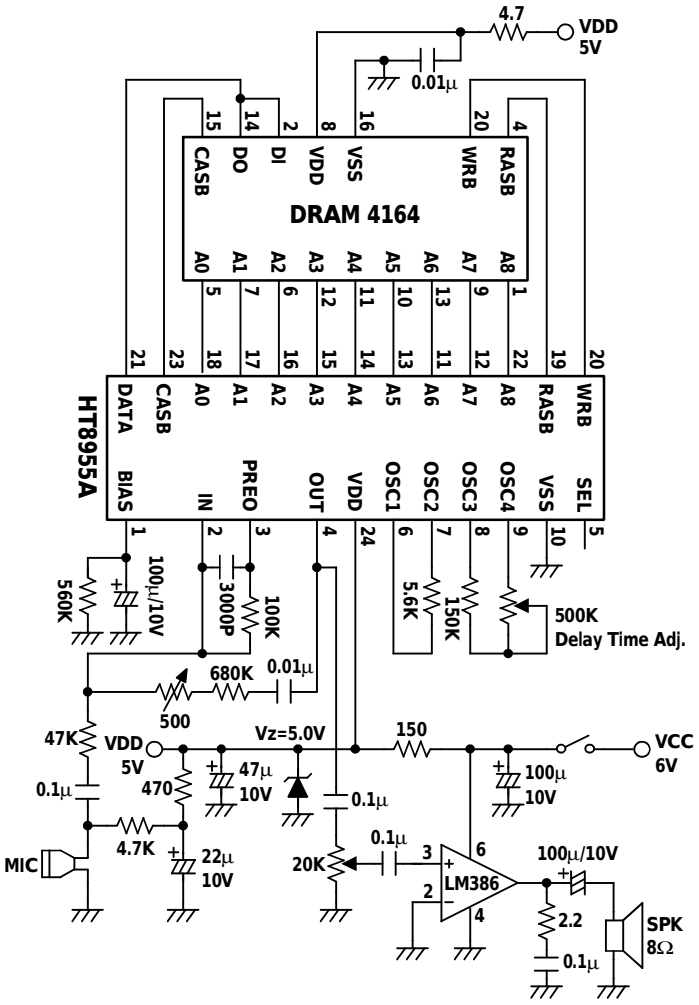
DRAM selection

The HT8955A can interface with a DRAM for storing delay signals. The type along with maximum delay time of DRAM is decided by the status of the SEL pin as shown:

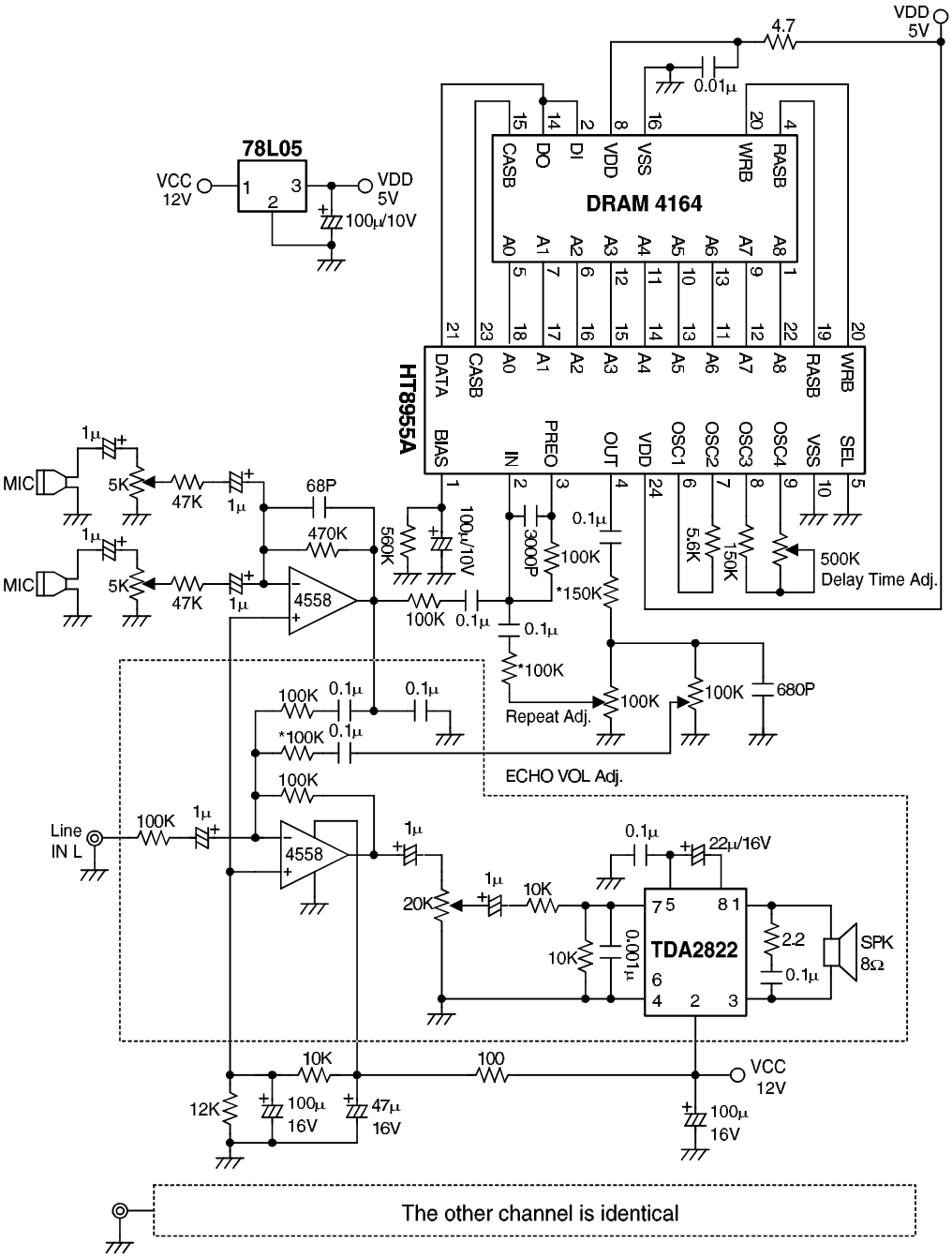
SEL Connection	DRAM Type	Delay Time
VDD or Open	64Kb	0.2 seconds
VSS	256Kb	0.8 seconds

Application Circuits

Low cost echo

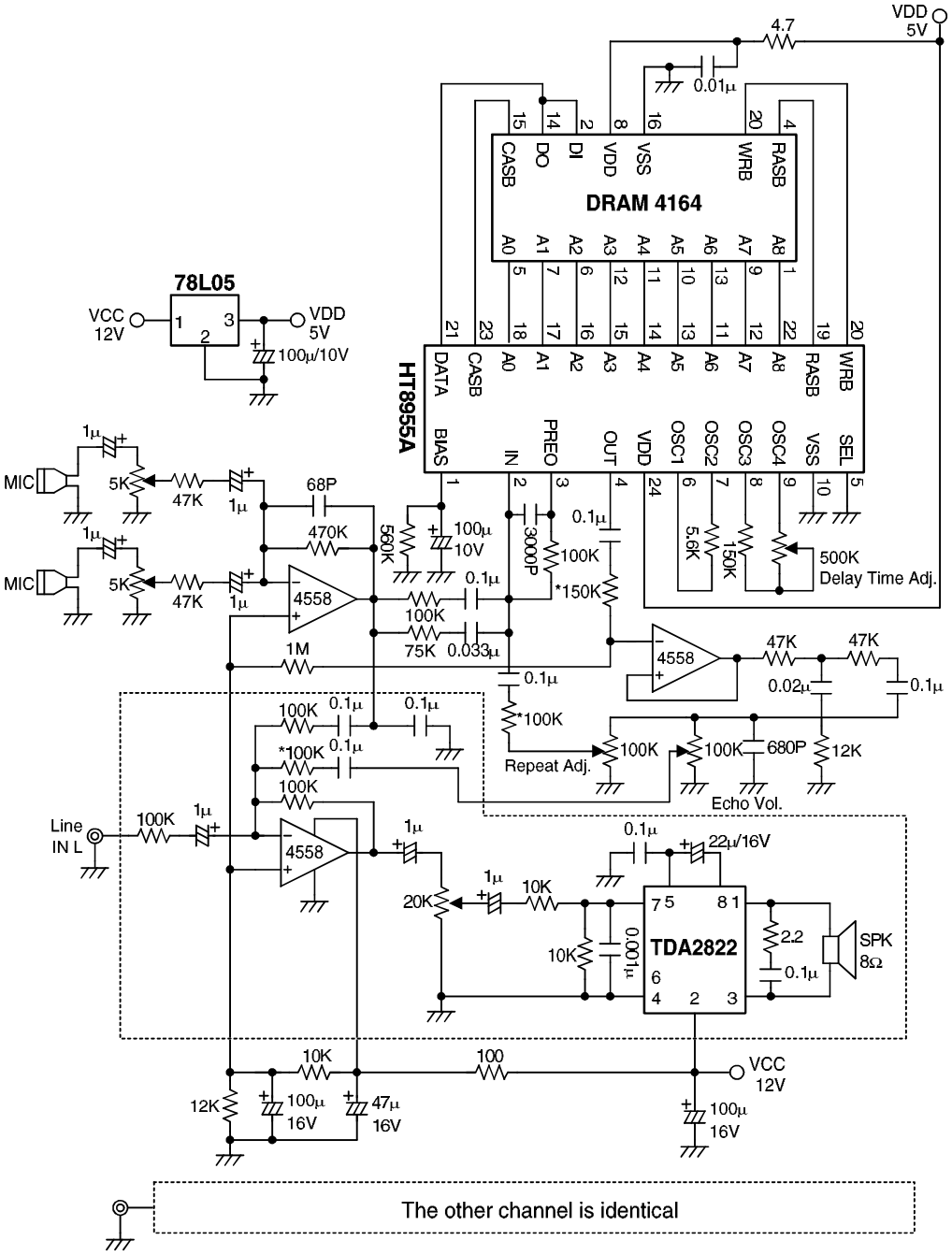


Basic KARAOKE system



*Note: In practical applications, the value of marked part may be adjusted to favorite effect.

Basic KARAOKE system with pre-emphasis



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