

MJW21195 (PNP) MJW21196 (NPN)

Silicon Power Transistors

The MJW21195 and MJW21196 utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

Features

- Total Harmonic Distortion Characterized
- High DC Current Gain – $h_{FE} = 20 \text{ Min @ } I_C = 8 \text{ A dc}$
- Excellent Gain Linearity
- High SOA: 2.25 A, 80 V, 1 Second
- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	250	Vdc
Collector-Base Voltage	V_{CBO}	400	Vdc
Emitter-Base Voltage	V_{EBO}	5.0	Vdc
Collector-Emitter Voltage – 1.5 V	V_{CEX}	400	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C	16 30	A dc
Base Current – Continuous	I_B	5.0	A dc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C	P_D	200 1.43	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	40	$^\circ\text{C/W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

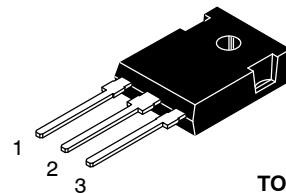
1. Pulse Test: Pulse Width = 5 μs , Duty Cycle $\leq 10\%$.



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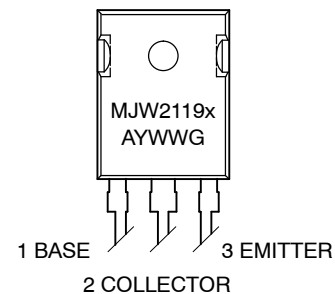
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**16 AMPERES
COMPLEMENTARY
SILICON POWER TRANSISTORS
250 VOLTS, 200 WATTS**



**TO-247
CASE 340L**

MARKING DIAGRAM



x = 5 or 6
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJW21195	TO-247	30 Units/Rail
MJW21195G	TO-247 (Pb-Free)	30 Units/Rail
MJW21196	TO-247	30 Units/Rail
MJW21196G	TO-247 (Pb-Free)	30 Units/Rail

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage ($I_C = 100 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	250	–	–	Vdc
Collector Cutoff Current ($V_{CE} = 200 \text{ Vdc}$, $I_B = 0$)	I_{CEO}	–	–	100	μAdc
Emitter Cutoff Current ($V_{CE} = 5 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	50	μAdc
Collector Cutoff Current ($V_{CE} = 250 \text{ Vdc}$, $V_{BE(off)} = 1.5 \text{ Vdc}$)	I_{CEX}	–	–	50	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased ($V_{CE} = 50 \text{ Vdc}$, $t = 1 \text{ s}$ (non-repetitive)) ($V_{CE} = 80 \text{ Vdc}$, $t = 1 \text{ s}$ (non-repetitive))	$I_{S/b}$	4.0 2.25	– –	– –	Adc
ON CHARACTERISTICS					
DC Current Gain ($I_C = 8 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$) ($I_C = 16 \text{ Adc}$, $I_B = 5 \text{ Adc}$)	h_{FE}	20 8	– –	80 –	
Base-Emitter On Voltage ($I_C = 8 \text{ Adc}$, $V_{CE} = 5 \text{ Vdc}$)	$V_{BE(on)}$	–	–	2.0	Vdc
Collector-Emitter Saturation Voltage ($I_C = 8 \text{ Adc}$, $I_B = 0.8 \text{ Adc}$) ($I_C = 16 \text{ Adc}$, $I_B = 3.2 \text{ Adc}$)	$V_{CE(sat)}$	– –	– –	1.0 3	Vdc
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output $V_{RMS} = 28.3 \text{ V}$, $f = 1 \text{ kHz}$, $P_{LOAD} = 100 \text{ W}_{RMS}$ (Matched pair $h_{FE} = 50 @ 5 \text{ A}/5 \text{ V}$)	T_{HD}		– –	0.8 0.08	– –
Current Gain Bandwidth Product ($I_C = 1 \text{ Adc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 1 \text{ MHz}$)	f_T	4	–	–	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f_{test} = 1 \text{ MHz}$)	C_{ob}	–	–	500	pF

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TYPICAL CHARACTERISTICS

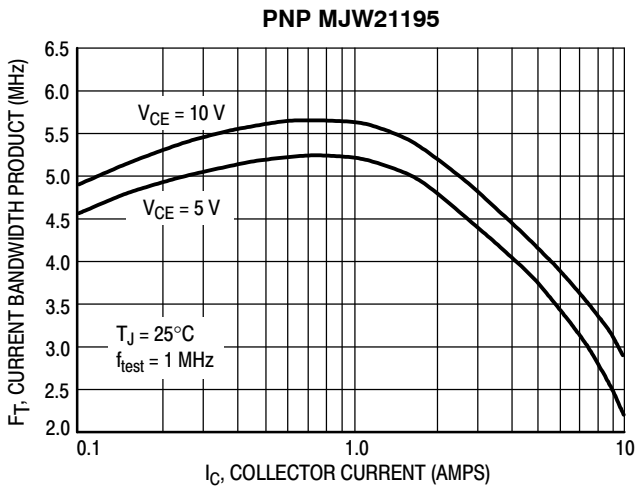


Figure 1. Typical Current Gain Bandwidth Product

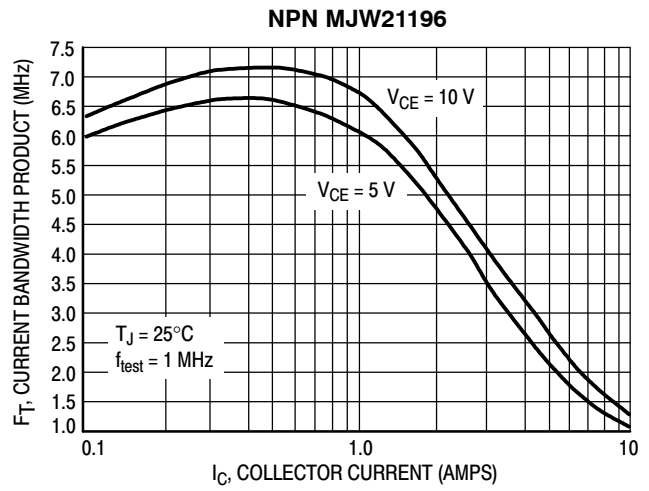


Figure 2. Typical Current Gain Bandwidth Product

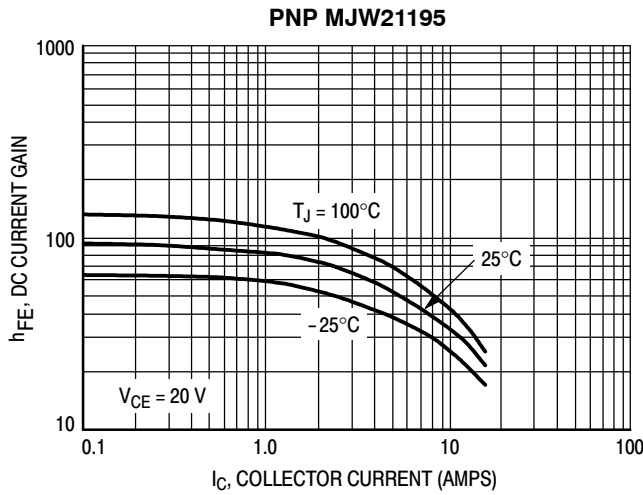


Figure 3. DC Current Gain, $V_{CE} = 20\text{ V}$

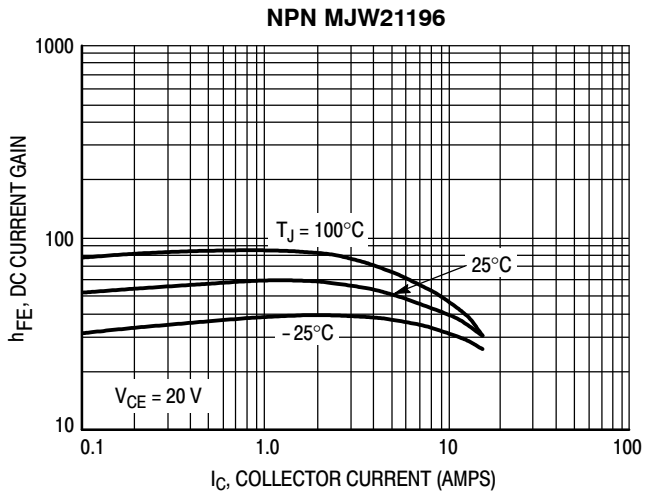


Figure 4. DC Current Gain, $V_{CE} = 20\text{ V}$

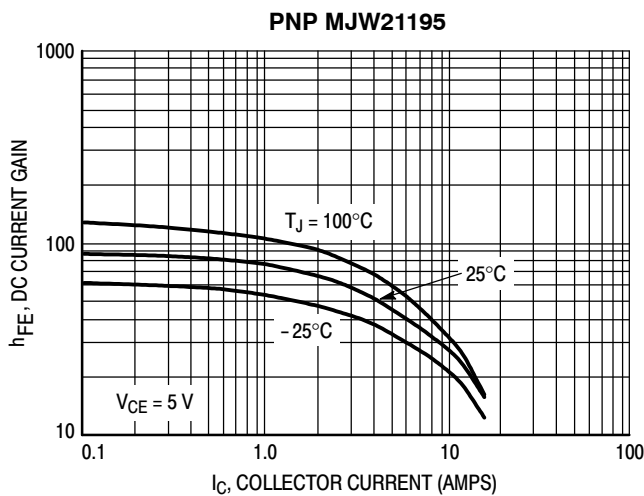


Figure 5. DC Current Gain, $V_{CE} = 5\text{ V}$

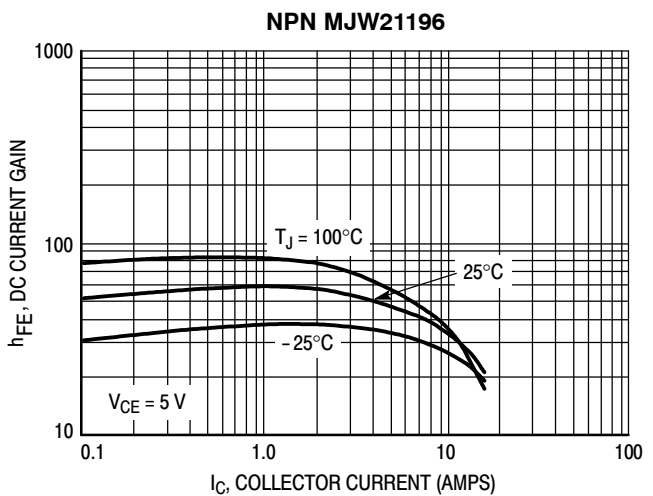


Figure 6. DC Current Gain, $V_{CE} = 5\text{ V}$

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TYPICAL CHARACTERISTICS

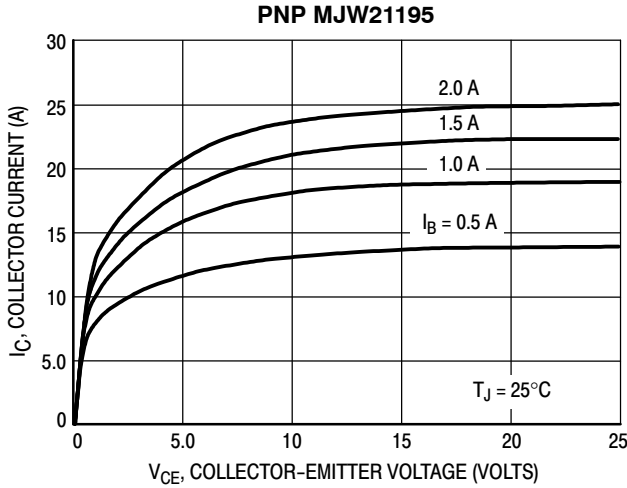


Figure 7. Typical Output Characteristics

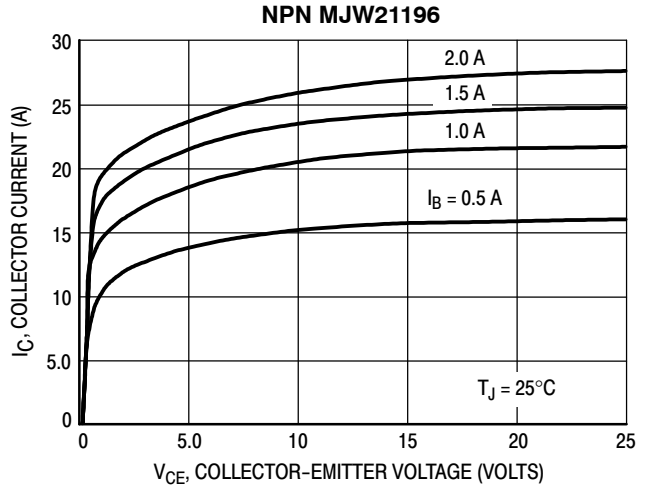


Figure 8. Typical Output Characteristics

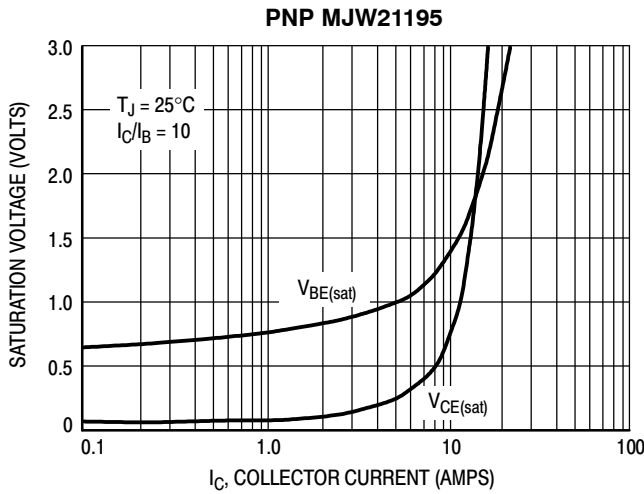


Figure 9. Typical Saturation Voltages

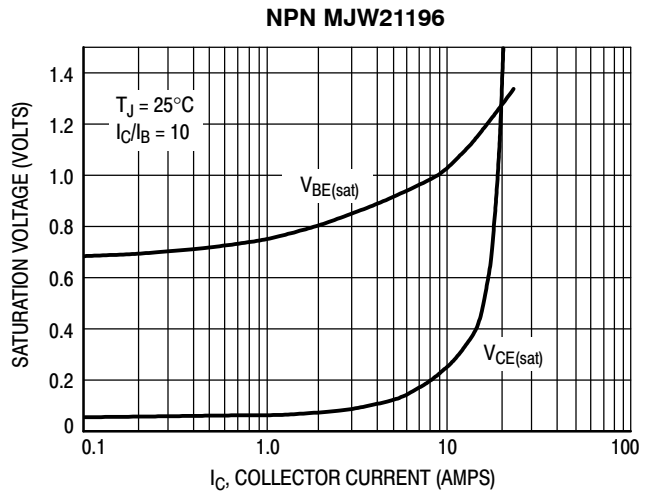


Figure 10. Typical Saturation Voltages

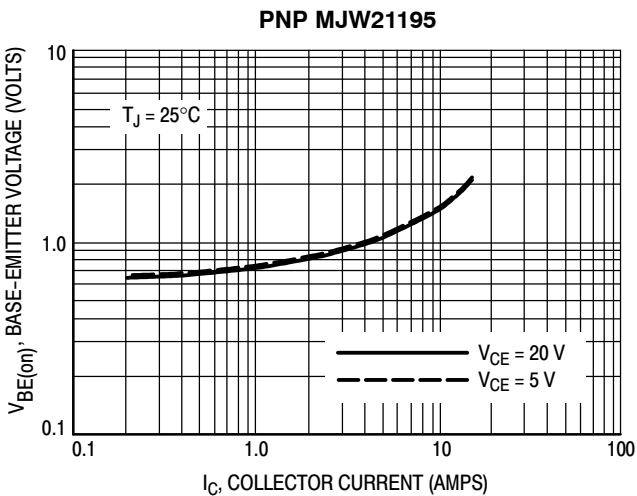


Figure 11. Typical Base-Emitter Voltage

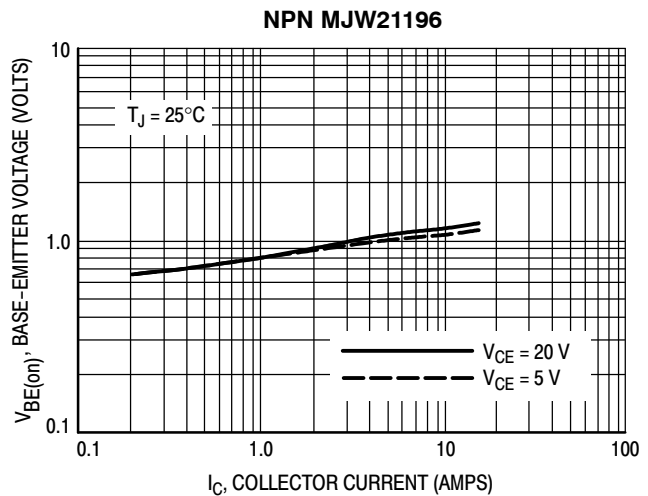


Figure 12. Typical Base-Emitter Voltage

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There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

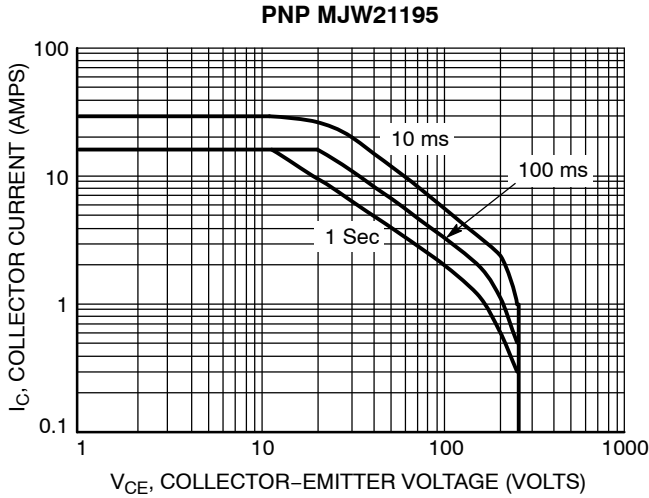


Figure 13. Active Region Safe Operating Area

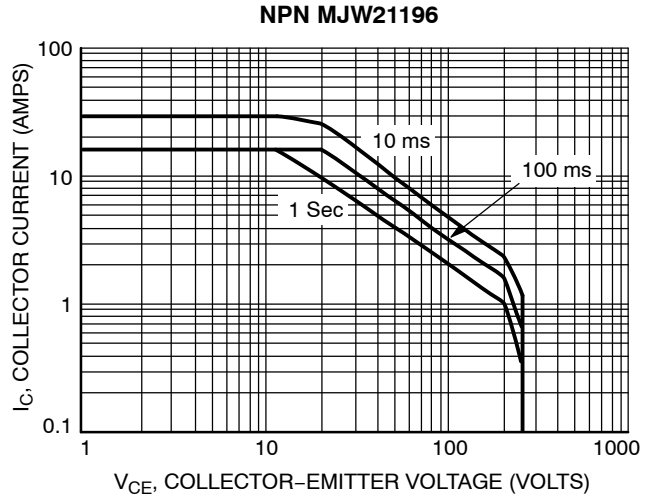


Figure 14. Active Region Safe Operating Area

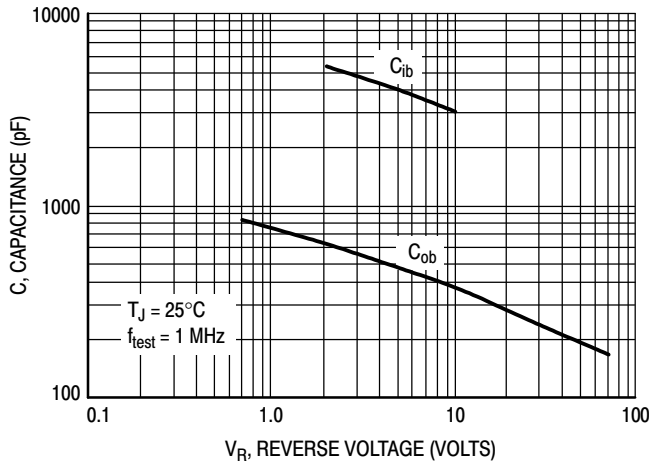


Figure 15. MJW21195 Typical Capacitance

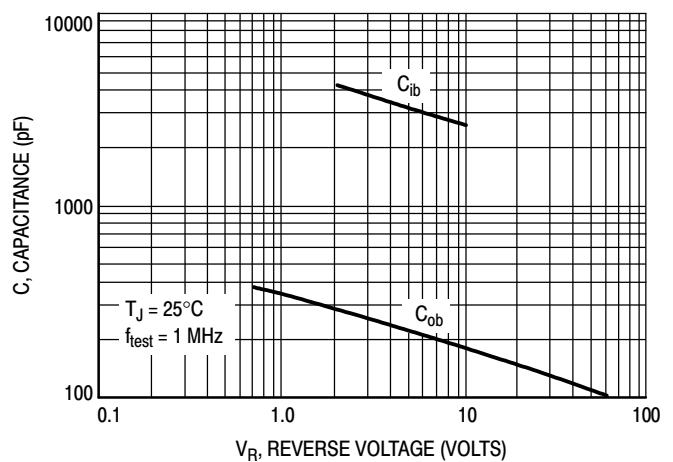


Figure 16. MJW21196 Typical Capacitance

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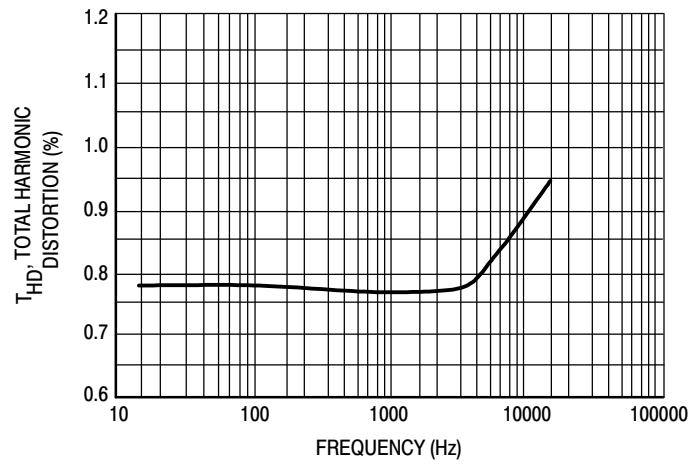


Figure 17. Typical Total Harmonic Distortion

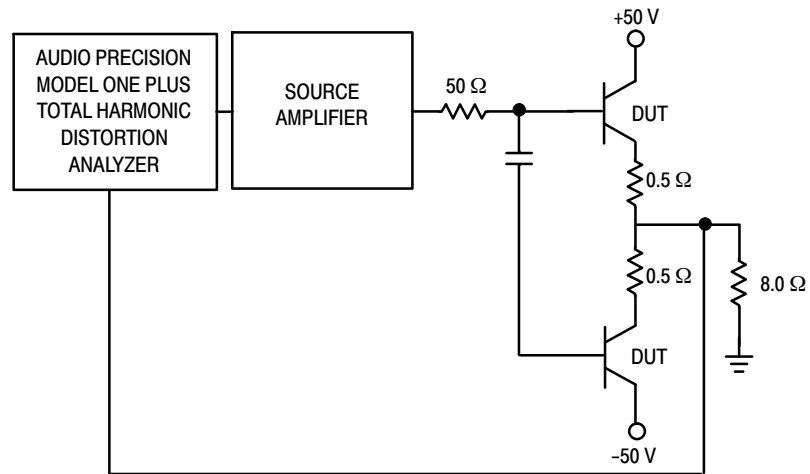
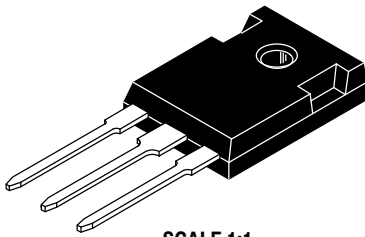


Figure 18. Total Harmonic Distortion Test Circuit

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

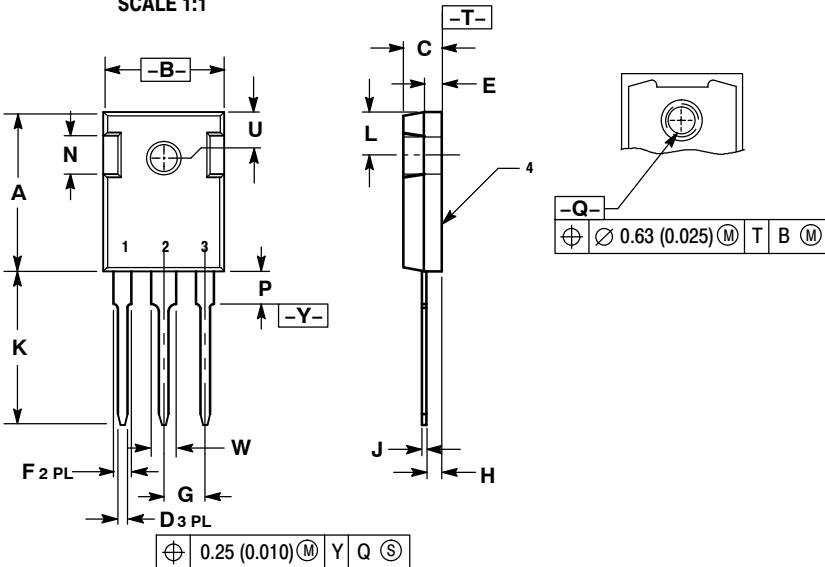
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TO-247
CASE 340L-02
ISSUE F

DATE 26 OCT 2011

SCALE 1:1

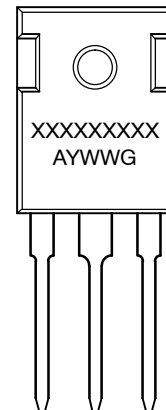


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	0.830
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

- STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)
- STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-247	PAGE 1 OF 2



ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80-21.46/0.819-0.845. DIM K WAS 19.81-20.32/0.780-0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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